RECENT PROGRESS IN WIDEBAND MONOLITHIC DIRECT DIGITAL SYNTHESIZERS

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ABSTRACT

This paper presents recent progress in the development of wideband monolithic GaAs DDSs, since its debut in 1992. A wideband DDS generates sinusoidal waveforms with several hundred megahertz of bandwidth, subhertz resolution and nanosecond frequency switching speeds. A discussion of improvements made to the monolithic GaAs HBT DDS and factors driving design and performance are presented.

INTRODUCTION

The design and application of wideband direct digital synthesizers (DDS) is a growing area of interest for the RF-microwave and signal processing community. Wideband DDSs are capable of generating sinusoidal waveforms with several hundred megahertz of bandwidth, nanosecond switching times, subhertz resolution and spurious-free dynamic range (SFDR) of better than -40 dBc. Wideband DDS devices are finding applications as local oscillators and modulators in a medley of radar, electronic warfare and communication systems[1].

Over the past 5 years, GaAs HBT technology has demonstrated a variety of monolithic DDS designs such as a linear-FM (chirp) synthesizer[2], a conventional DDS[3], and a serrodyne modulator[4]. These designs have focused on integrating digital and analog circuitry monolithically to achieve highest performance over hybrid or discrete approaches. This performance improvement can be characterized as smaller size and weight as well as low power and cost.

Since the first development of monolithic GaAs DDSs, several technical advancements have been made toward improving their performance parameters. These improvements were obtained with a combination of GaAs HBT process and design changes. The process changes involved modifying the HBT epitaxial structure to provide better linear performance for analog operation without degrading performance for the high-density, I^2L-like digital circuitry. As has been discussed within DDS developer circles, the digital-to-analog conversion (DAC) process is far from ideal. Most design improvements over the years have focused on improving the SFDR of the DAC and increasing the DDS's clock speed (operating bandwidth). One improvement developed for reducing glitch energy is utilizing a feed-back loop to control the glitching mechanism within the DAC's bit-switch register[5].

CIRCUIT DESCRIPTION

A block diagram of the monolithic DDS is shown in Figure 1, and is essentially identical to the first monolithic GaAs DDS reported in 1992[3]. The accumulator subcircuit is made up of a 32-bit pipelined accumulator, 12-bit pipelined phase adder and registers for holding frequency and phase control words. Two small controllers on-chip handle frequency and phase control word changes. Each clock cycle, 32 bits of

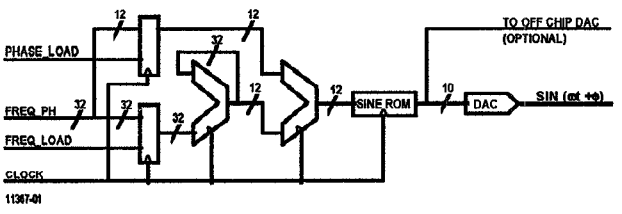

Figure 1. DDS Block Diagram

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instantaneous phase data is created by the accumulator and the 12 most significant bits (MSBs) are added to the contents of the phase control word register. Upon leaving the phase adder, the data is time-aligned and handed off to the sine look-up ROM.

The sine look-up ROM stores one quadrant of a sinusoidal waveform in a reduced-data format using trigonometric identities. The 10 least significant bits (LSBs) of the phase word address the appropriate 9-bit sine value with the two MSBs of the phase word being used to identify the sign and quadrant of the generated waveform. The resultant 10-bit sine value represents the instantaneous amplitude of the sinewave for a given clock period. This 10-bit word is then transferred to the on-chip DAC before release off chip.

The 10-bit DAC is a segmented architecture, that combines a conventional 6-bit R/2R DAC and a 15-level unitary DAC to provide the analog output. A block diagram of the on-chip DAC is shown in Figure 2. Schottky diodes are used to steer the bit current from the DAC output or from the switch driver depending on the state of the controlling bit. The segmented architecture combines the R2/R and unitary DAC circuits into a coarse/fine arrangement with the unitary DAC generating coarse steps and the R2/R DAC providing the fine steps. The combination of 16 coarse levels and 64 fine levels results in a total of 1024 output levels or 10-bits of resolution.

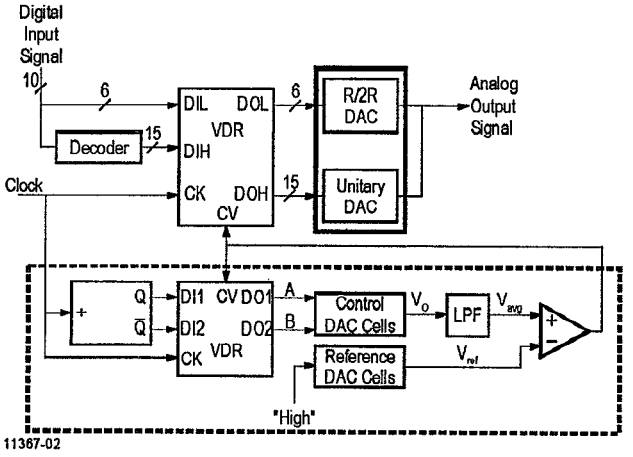

Figure 2. On-Chip DAC Block Diagram

DESIGN AND TECHNOLOGY IMPROVEMENTS

A photograph of the most recent monolithic GaAs DDS is shown in Figure 3. Since its inception, the primary focus of development for the DDS has been in improving speed (increasing tuning bandwidth) and spurious performance. Improvements in both of these areas have been demonstrated as a result of changes to the DDS design and fabrication.

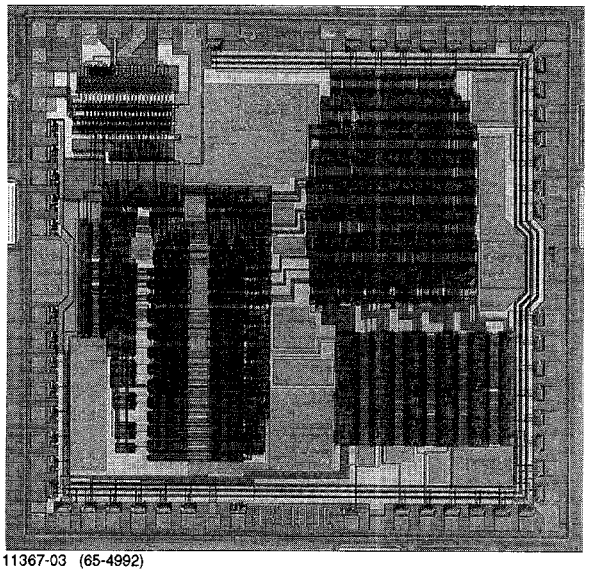

Figure 3. Monolithic GaAs DDS

In general, most of the major spurs in the DDS are due to nonlinearities associated with the digital to analog conversion process. A major cause of distortion in the analog output of a DAC is the skew in the on and off switching times of the DAC bit currents. Perhaps the best known example is the glitch that results when attempting to simultaneously turn some bit currents on and others off. A glitch occurs if all of these bit currents are momentarily on, causing larger than expected output current, or off, causing less than expected output current, before reaching their final states.

A method[5] demonstrated in the DDS for minimizing this distortion involves a glitch control loop, which uses a pair of DAC cells (switched out of phase) to generate a control voltage proportional to the skew in the bit current switching times. A block diagram of the on-chip DAC is shown in Figure 2. The control voltage is used in a pair of register cells to control the alignment of the rising and falling edges of switching waveforms A and B as shown in Figure 2. The resulting negative feedback system forces an alignment of signals A and B that produces minimum glitch distortion. The same control voltage is then used in a DAC made up of identical components (portion above dotted line) to achieve minimum switching skew distortion. With the exception of the low-pass filter, the entire feedback loop is integrated on chip in the DAC.

When the first monolithic DDS was demonstrated in 1992, the GaAs HBT technology used was primarily intended for digital integration. Two analog co-integration limitations were common-emitter only transistor structures and very low Early voltage, a parameter for linearity. GaAs HBT/HI^{2}L collector-up transistors are connected on an n+ substrate allowing contact to the backside for the common emitter. In this fashion, high density logic designs are possible where the delay-power product of the device is at a premium. To achieve this low product, the device is built for small size and planarity. However, analog circuit capability is limited.

Recently, improvements to the device have been made to enhance mixed-signal performance. The base sheet resistance has been reduced by converting from an implanted base, similar to silicon processing methods, to an epitaxially grown base, whereby carbon doping is used in MOCVD layer deposition. Sheet resistance is in the 2,000- to 5,000-ohm/square range for the grown base devices, and is in the 400-ohm/square range for advanced GaAs devices. Another benefit from the grown base device is that the collector doping adjacent to the base can be lowered, as in conventional devices, and collector base capacitance reduced. The combination of base and collector improvements raises the Early voltage, providing a current gain-Early voltage product of 2,000, which has a favorable impact on analog operation within the DDS's DAC. Advanced GaAs HBT/HI^{2}L devices under development have a product as high as 20,000.

Switching to a grown-base device has provided a 3-percent improvement in transistor switching speed allowing the DDS to demonstrate clock speeds of 1.0 GHz. The end result is a switching speed of 50 ps at 1 mW for a fanout = 1 baseline device, and a 25-ps speed at 1 mW for the advanced device. Future improvements will depend on the ability to further shrink the device to one square micron per collector.

TEST RESULTS

The DDS IC has demonstrated its design goal of 800-MHz clock operation with a maximum clock speed of 1.0 GHz. This improvement is a direct result of switching from the implanted base to a grown base transistor structure. Furthermore, this change allowed improvements in Early voltage, which when coupled with the new DAC design, enabled lower spurious operation.

The best way to demonstrate these improvements is by doing an "apples-to-apples" comparison of the 1992 DDS to the recently improved DDS. Figure 4 shows a plot from a spectrum analyzer of a 109.35-MHz output from the 1992 monolithic DDS. The worst-case spur for this example was -38 dBc at a DDS clock rate of 500 MHz. By comparison, Figure 5 shows a plot from a

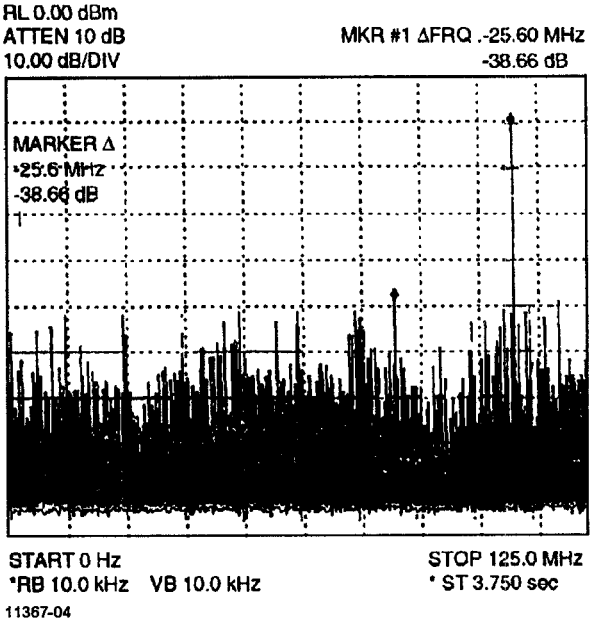

Figure 4. Spectrum of 109.350-MHz Output from DDS/M Chip

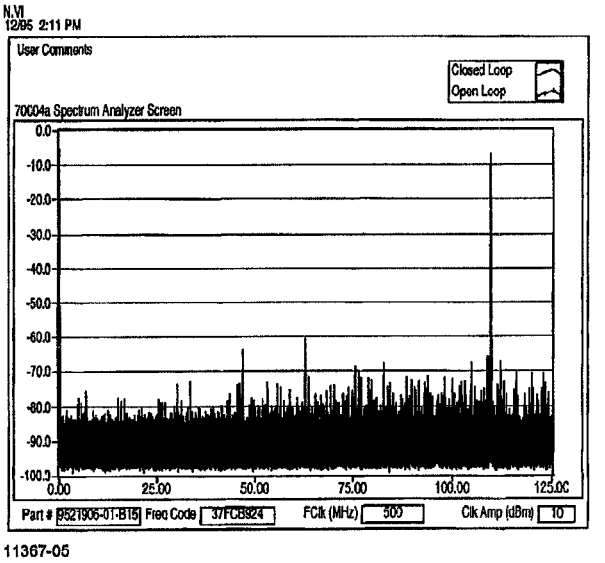

Figure 5. Spectrum of 109.350-MHz Output from DDS/M Chip and Worst-Case Spur of -54 dBc

spectrum analyzer of the same conditions (F_{clock} = 500 MHz, F_{out} = 109.35) and a worst-case spur of -54 dBc. Table 1 compares the two device.

TABLE 1. COMPARISON OF 1992 AND 1995 GaAs DDS

	1992 GaAs DDS	1995 GaAs DDS
Designed clock rate	500 MHz	800 MHz
Clock F-max	660 MHz	1000 MHz
Worst-case spur (F_{clock} = 500 MHz, F_{out} = 109.35 MHz)	-38 dBc	-55 dBc
Power dissipation	4.5 W	5.8 W
Die size	3.8 × 4.1 mm	3.0 × 3.2 mm

A DDS's worst case spur at wideband (Nyquist bandwidth = DC to $F_{clock}/2$) typically occurs when the output frequency is tuned to a frequency close to $F_{clock}/3$. Figure 6 shows the worst case spur for the current monolithic DDS at a clock frequency of 800 MHz, and an output frequency of 256.25 MHz. The worst case spur is the aliased second harmonic at 287.5 MHz. This spur will cross the output frequency as the DDS tunes higher in frequency and as such represents a problem for systems demanding lower spur performance. Usually, frequency synthesizer designers apply the DDS around these worst-case spurs. Elimination of this spur from the DDS is the focus of current work with MIT Lincoln Laboratory and will allow larger tuning bandwidths with spurious free dynamic range in excess of 50 dB.

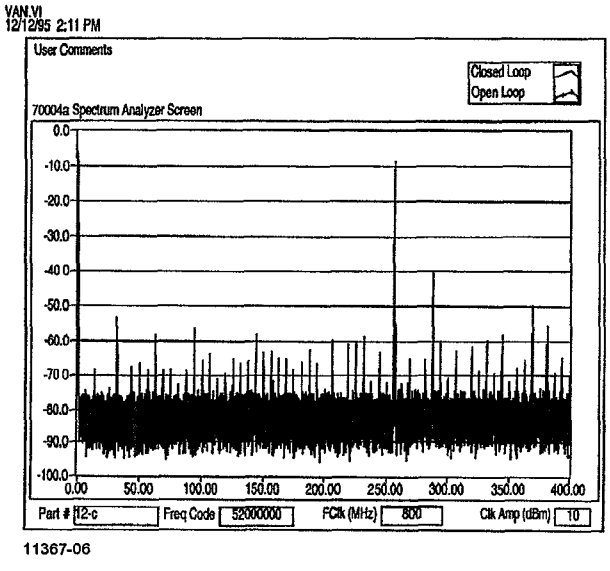

Figure 6. Worst-Case Spur for Current Monolithic DDS at a Clock Frequency of 800 MHz

CONCLUSIONS

In conclusion, we have described recent results in the development of a wideband monolithic DDS. Improvements in both design and GaAs HBT wafer technology have provided gains in speed and SFDR. On-going work in advanced design and wafer technology hold promises of higher speeds with lower spurious and power dissipation.

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